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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,538	06/10/2005	Dennis Ciplickas	524322000300	4236

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EXAMINER	
ANYA, IGWE U	

ART UNIT	PAPER NUMBER
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,538	CIPLICKAS ET AL.	
	Examiner	Art Unit	
	Igwe U. Anya	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/19/05, 6/13/07,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 - 2, 5, 12 -15, 28, 29, 32, 37, 39 - 42, and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by So et al. (US Patent 5,831,446).

3. So et al. teach a method for fast localization of electrically measured defects of integrated circuits, comprising:

(a) obtaining a test chip (120) fabricated to have test structures configured for parallel electrical testing (fig. 3A);

(b) electrically testing the test structures on the test chip employing a parallel electrical tester (col. 4 lines 4 – 62); and

(c) analyzing results of the electrical testing to localize defects on the test chip (col. 4 lines 46 – 51).

further comprising inspecting the localized defects on the test chip using an inspection tool (col. 2 lines 36 – 39);

in-line inspecting the test chip using an optical inspection tool (col. 4 lines 52 - 62);

wherein the test chip includes a plurality of design pattern variations (col. 2 lines 27 - 44);

wherein the test structures are two-terminal or four terminal test structures (col. 2 lines 36 - 39);

wherein analyzing results comprises classifying detected defects as random or systematic defects (col. 4 lines 52 - 62);

grouping test chip design patterns into layout bins, and plotting failure counts for each layout bin (col. 4 lines 52 - 62);

wherein one of the test structures is a snake comb cell configured to localize a defect in the snake comb cell to a location within the snake comb cell (fig. 1);

wherein the test structures are grouped into one or more pad groups, and the test structures in a pad group are electrically tested together in parallel (fig. 1);

wherein a pad group includes two columns of test structures, and two columns of pads disposed between the two columns of test structures (fig. 1); and

wherein pad groups are grouped into one or more sticks, wherein the pad groups in a stick are electrically tested together in parallel (col. 2 lines 61 - 67).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3, 4, 30, 31, and 43 - 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over So et al. (US Patent 5831446) in view of Chou et al. (US Patent 6291254).

So et al. teach the features previously outlined and probing the cells (col. 2 lines 36 - 39), but lacks:

the inspection tool being a scanning electron microscope (SEM);

sizing the test structures on the test chip to be compatible with a view field of the

SEM;

wherein the test structures are placed at more than one level;

wherein test structure below a test structure on another level is electrically tested; and

wherein the interaction of test structures at two different levels is measured.

8. However, Chou et al. teach determining interconnect parameters, comprising;

the inspection tool being a scanning electron microscope (col. 10 lines 60 -66);

sizing the test structures on the test chip to be compatible with a view field of the SEM (col. 11 lines 3 - 25).

wherein the test structures are placed at more than one level (fig. 4);

wherein test structure below a test structure on another level is electrically tested (col. 10 lines 9 - 11); and

wherein the interaction of test structures at two different levels is measured (col. 10 lines 14 - 52).

9. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Chou et al. into the So et al. reference to probe a pad as conventional in the art.

10. Claims 6 - 11, 18 - 20, 33 - 38, and 48 - 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over So et al. (US Patent 5831446) in view of Yamada et al. (US Patent 5666049).

11. So et al. teaches the features previously outlined, but lacks:

wherein a pad group includes two columns of test structures, and two columns of pads disposed between the two columns of test structures;

grouping pad groups into one or more sticks, wherein the pad groups in a stick are electrically tested together in parallel;

wherein the pad groups in a stick are electrically tested together in parallel using a probe card connected to the parallel electrical tester;

wherein the parallel electrical tester is connected to a wafer loader and a wafer prober, and further comprising: loading one or more test chips from the wafer loader into the wafer prober to be tested, and wherein the wafer prober includes a probe card to electrically contact the test structures on the test chip to be electrically tested in parallel;

transmitting test signals between the probe card and a pin termination module in the parallel electrical tester; transmitting test signals between the pin termination module and a measurement control module in the parallel electrical tester;

transmitting commands to the wafer prober from a tester control module in the parallel electrical tester; and

transmitting voltage sources and control signals from the measurement control module to the pin termination module.

12. However, Yamada et al. teach:

wherein a pad group includes two columns of test structures, and two columns of pads disposed between the two columns of test structures (fig. 14A) ;

grouping pad groups into one or more sticks, wherein the pad groups in a stick are electrically tested together in parallel (fig. 14A);

wherein the pad groups in a stick are electrically tested together in parallel using a probe card connected to the parallel electrical tester (fig. 14A);

wherein the parallel electrical tester is connected to a wafer loader and a wafer prober, and loading one or more test chips from the wafer loader into the wafer prober to be tested, and wherein the wafer prober includes a probe card to electrically contact the test structures on the test chip to be electrically tested in parallel (fig. 12);

transmitting test signals between the probe card and a pin termination module in the parallel electrical tester (fig. 17); transmitting test signals between the pin termination module and a measurement control module in the parallel electrical tester, and transmitting commands to the wafer prober from a tester control module in the parallel electrical tester (fig. 17); and

transmitting voltage sources and control signals from the measurement control module to the pin termination module (fig. 5).

13. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Yamada et al. into the So et al. reference to probe a cell using a probe card in parallel testing.

14. Claims 16, 17, 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over So et al. (US Patent 5,831,446) in view of Hess et al. (UPAP 2004/0094762).

15. So et al. teach the features previously outlined but, lack:

wherein electrically testing includes:

comparing a line resistance to a first threshold resistance, wherein the line resistance is determined based on a measured voltage;

when the line resistance is below the first threshold voltage, detecting a soft short;

comparing the line resistance to a second threshold resistance; and

when the line resistance is below the second threshold resistance, detecting a hard short, wherein the first threshold resistance is greater than the second threshold resistance.

wherein electrically testing includes:

determining an average resistance for a number of lines adjacent to each other;

comparing a line resistance to the average resistance;

when the line resistance is less than the average resistance by a first specified amount, detecting a soft short; and

when the line resistance is less than the average resistance by a second specified amount, detecting a hard short, wherein first specified amount is less than the second specified amount.

16. However, Hess et al. teach:

wherein electrically testing includes comparing a line resistance to a first threshold resistance, wherein the line resistance is determined based on a measured voltage (paragraph 58 – 69);

wherein, when the line resistance is below the first threshold voltage, a soft short is detected (paragraphs 70 – 81);

comparing the line resistance to a second threshold resistance, and when the line resistance is below the second threshold resistance, a hard short is detected, and wherein the first threshold resistance is greater than the second threshold resistance (paragraphs 82 – 89);

wherein electrically testing includes determining an average resistance for a number of lines adjacent to each other, and comparing a line resistance to the average resistance, and

wherein, when the line resistance is less than the average resistance by a first specified amount, a soft short is detected (paragraphs 90 – 93); and

wherein, when the line resistance is less than the average resistance by a second specified amount, a hard short is detected, and wherein the first specified amount is less than the second specified amount (paragraph 94), for the benefit of improving accuracy of determining defect size distributions and defect size densities .

17. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Hess et al. into the So et al. reference for the benefit of improving accuracy of determining defect size distributions and defect size densities.

18. Claims 21 - 25, and 51 - 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over So et al. (US Patent 5831446) in view of Yamada et al. (US Patent 5666049), and further in view of Kim et al. (US Patent 6323664).

19. The So/Yamada et al. reference teaches the features previously outlined, but

lacks:

receiving test signals from the probe card at a plurality of switch cards in the pin termination module, wherein each switch card is, connected to a group of pins from the probe card;

wherein a switch card forms a resistor divider with a resister in a test structure, a termination resistor, and a voltage source;

wherein a switch card includes a plurality of pin terminator circuits, each pin terminator circuit is connected to a pin from the probe card and a plurality of digital multiplexer controls (MUX0 - MUX31), and each digital multiplexer control is connected to two pin terminator circuits;

wherein a pin terminator circuit includes a plurality of quad switches (ϕ1 - ϕ4), and each quad switch is connected to a voltage source and control signals; and

receiving test signals from the probe card at a multiplexer module in the measurement control module, combining a set of test signals received from the probe card into a digital acquisition signal, and transmitting the digital acquisition signal to a digital acquisition card (fig. 4).

20. However, Kim et al. teach:

receiving test signals from the probe card at a plurality of switch cards in the pin termination module, wherein each switch card is, connected to a group of pins from the probe card (fig. 3);

wherein a switch card forms a resistor divider with a resister in a test structure, a termination resistor, and a voltage source (fig. 4);

wherein a switch card includes a plurality of pin terminator circuits, each pin terminator circuit is connected to a pin from the probe card and a plurality of digital multiplexer controls (MUX0 - MUX31), and each digital multiplexer control is connected to two pin terminator circuits (fig. 3);

wherein a pin terminator circuit includes a plurality of quad switches (ϕ1 - ϕ4), and each quad switch is connected to a voltage source and control signals (fig. 4); and

receiving test signals from the probe card at a multiplexer module in the measurement control module, combining a set of test signals received from the probe card into a digital acquisition signal, and transmitting the digital acquisition signal to a digital acquisition card (fig. 4).

21. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Kim et al. into the So/Yamada et al. reference to accurately test defective cells.

22. Prior art made of record and not relied upon, considered pertinent to applicant's disclosure are listed in PTO-892 Form.

Contact Information

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M - F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on (571) 272-1722. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Art Unit 2891

IA

August 1, 2007